REMARKS

Claims 1-13, 16-23 and 25-27 are currently active.

The Examiner has rejected Claims 1-4 and 16 as being unpatentable over Sutardja in view of Powell. Applicants respectfully traverse this rejection.

Referring to Sutardja, there is disclosed a high latency timing circuit. Sutardja teaches the timing circuit for synchronization of phase and frequency, and particularly to such a circuit having a highly pipelined structure. Sutardja teaches if the channel is to be operated at a high-speed, the feedback loop must be structured in a highly pipelined manner; i.e., more feedback elements must be present in the loop. This causes the loop to have a high latency, or time delay, associated with it. The high latency generally causes a degraded performance of the timing loop, which in turn requires that the loop of bandwidth be reduced in order to maintain loop stability. However, the timing acquisition must be accompanied in as short a time as possible, in order to maintain the speed of the channel and thereby not adversely impact overall system performance. Thus, a dilemma for implementation of high speed channels is presented. See column 1, lines 50-62.

To overcome this, Sutardja teaches a high-speed timing recovery system with reduced latency. The system that Sutardja teaches addresses the need for more effective timing recovery circuits to be used in high-speed channels, such as a read channel and a hard disk drive. See column 5, lines 35-37. Sutardja teaches that a timing circuit can be viewed as a type 1 timing circuit, in which only phase correction occurs, or a type 2 timing circuit, in which both phase correction and frequency correction occur. In a type 1 circuit, because only phase correction occurs, the frequency integration feedback loop need not be operational. Thus, in a type 1 circuit, a higher loop bandwidth and correspondingly higher speed are possible, as compared to a type 2 circuit having the same latency, because a type 1 circuit inherently is more stable than a type 2 circuit. The type 2 circuit can be used as a type 1 timing circuit by disabling the frequency integration feedback loop. This may be achieved by setting the input to the frequency integration feedback loop equal to 0. In this manner, a high bandwidth type one circuit can operate to lock onto the correct timing of phase. However, because no frequency correction occurs, there is still a significant timing frequency error. Such an uncorrected timing frequency error will eventually cause the timing circuit to fail, after the channel switches from acquisition mode to tracking mode. Sutardja teaches to use the type 1 circuit while in the acquisition mode, and simultaneously calculate an estimated value of frequency offset. By calculating the estimated frequency offset while in the acquisition mode, the timing frequency can be adjusted prior to exiting acquisition mode and entering checking mode. See column 5, lines 35-65.

Sutardja teaches that first, during the acquisition mode period, operate the type 1 circuit at a high bandwidth value to lock onto the timing phase and calculate the frequency offset. Then, enable the frequency integration feedback loop, thereby converting the circuit into a type 2 circuit, by resetting it's input so that the input is equal to the calculated frequency offset value. Finally reduce the bandwidth to a low value so that the type 2 circuit can operate in tracking mode while maintaining stability of the timing circuit. The frequency offset is calculated by the type 1 circuit by taking 2 phase measurements at the output of the phase integration feedback loop, subtracting the first value from the second, and dividing the difference by the elapsed time. See column 6, lines 1-12.

Sutardja teaches that the implementation of such a timing circuit is the use of a digital loop filter 200 and a phase-locked loop circuit. The digital loop 200 includes 2 integrators 205, 210. The first integrator 205 is the timing frequency integrator, and the second integrator 210 is the timing phase integrator. The target signal 215, i.e., the signal being communicated via the channel and requiring timing recovery, is one input to the frequency integrator 205. The frequency correction gain parameter acts as a second input 220 to the frequency integrator 205 and is denoted by the variable b. The multiplier 225 combines the inputs 215 and 220 to produce another version of the signal which has the same characteristics as 215, except that its magnitude is controlled by 220. This result enters the feedback loop by an adder 230. The multiplexer 235 combines in an output of the phase shift

measurement circuit 240. The delay element 245 operates on the result of multiplexing the magnitude control signal with the phase shift measurement, and the output of the delay element 245 is fed back to the adder 230. By adding the delayed version of the magnitude-controlled signal with the underlying undelayed version of the magnitude-controlled signal an estimate of the frequency offset is made. See column 6, lines 13-36.

Sutardja teaches if the frequency integrator 205 is enabled by setting the input gain 220 to some non-zero value, the phase-locked loop circuit 200 is running in type 2 mode. However, if the phase correction gain 255 is sufficiently large, as in the typical case during the acquisition 105, the loop 200 can still function properly while the frequency integrator 205 is disabled. This will allow circuit 200 to run in type 1 mode. See column 6, lines 60-column 7, line 2. Once the frequency of said value 430 is calculated, the frequency integrator 205 can be enabled by setting the input frequency correction gain parameter 220 to that value. Thus, higher stability for the timing loop 200 is achieved during acquisition 105, while effectively providing frequency correction capability that is normally provided by a type 2 timing circuit. See column 7, lines 11-17.

From the above discussion, it is clear the hole purpose and intent of the teachings of Sutardja is to use a type 1 timing circuit as a type 2 timing circuit. See column 5, line 50. All the elements taught by Sutardja such as the frequency integrator 205, have the simple and straightforward definition set out in Sutardja itself. The context in these teachings

cannot be ignored. The interpretation the Examiner is applying to these elements is pure speculation. It is respectfully submitted, the Examiner is using hindsight to apply the limitations of applicants' invention of Claim 1 to the elements taught by Sutardja. The Examiner is reading these limitations into the teachings of Sutardja, where they are not present at all. Accordingly, Sutardja does not teach the limitation of a first filter for removing jitter from the signal and a second filter for removing wander from the signal separate and apart from the first filter.

It is respectfully submitted that a review of column 6, lines 13-52 of Sutardja does not teach or suggest any type of filtering for jitter or filtering for wander. The Examiner admits that this is his interpretation. The Examiner is reading limitations of the claims in Sutardja where they are just not there. In fact, in the context of the teachings of Sutardja, it is for a high-speed timing recovery system with reduced latency. See column 1, lines 66 and 67. The purpose of the phase locked circuit that the Examiner relies on in column 6, lines 13-52 is for high-speed timing recovery with reduced latency period. The Examiner teaches that the timing circuit can be viewed as either a type I timing circuit, in which only phase correction occurs, or a type II timing circuit, which both phase correction and frequency correction occur. See column 5, lines 40-44. The Examiner is reminded that under patent law, teachings cannot be taken of the context in which they are found. It is respectfully submitted that the Examiner is doing exactly that when he is interpreting the filters taught by Sutardja as being for wander and jitter.

In regard to the reference by incorporation to Powell, this is found in the background of the invention of Sutardja where 13 patents are cited, only for the proposition that they are phase-locked loop timing circuits. When reviewing Powell and column 1, lines 31-44, this is again part of the background of the invention of Powell. It simply identifies that jitter and wander are critical to the performance of a Sonet. It does not teach or suggest anything further in regard to filtering of jitter and wander. In fact, the purpose and context of Powell is to deal with the slow response times to phase changes, significant phase drift or MTIE that may occur in a Sonet network during holdover recovery. See column 2, lines 5-12. Basically, Powell teaches to acquire a second frequency from a first frequency of a reference signal with a phase locked loop 24. After the frequency is acquired, the interval register 39 of the phase locked loop 24 is loaded with the contents of the output frequency registers 34 of the phase locked loop 24. The phase detector 28 of the phase locked loop 24 is then realigned to the reference signal. To reiterate, there is no specific teaching or suggestion with respect to wander or jitter in Powell.

Powell teaches a method and apparatus for achieving fast phase settling in a phase locked loop upon a frequency change in the reference signal and more specifically for fast phase settling during the clock hold over recovery period in a synchronous optical network. Powell teaches that because phase locked loops normally used in Sonet network elements have slow response times to phase changes, significant phase drift or MTIE may

occur in the network element clock output during holdover recovery. See column 2, lines 6-12.

Powell teaches a Sonet network 10 comprises network elements 12 and fiber optic transmission medium 14. The network elements 12 receive payload signals from one or more sources. Network elements 12 synchronize the optical carrier to a synchronization reference signal received from a network provider synchronization network. Each network element 12 generates its optical carrier transmit frequency based on the output frequency of its network element clock.

Powell teaches in operation, phase locked loop 24 operates similarly to existing second order digital phase locked loops when the frequency of the reference signal remains fairly stable. When a relatively significant change in the frequency of the reference signal occurs, however, phase locked loop 24 achieves fast phase settling. The network element clock has acquired the new frequency at time T1. Powell teaches his invention seeks to maintain the phase difference between the reference signal and the network element clock at time T1. In many applications, such as in a Sonet network element clock, the phase of the clock only needs to be locked relative to the phase of the reference signal. It is not required to be locked in the specific absolute phase difference. Powell teaches to adjust the phase locked loop so as to maintain the relative phase difference between the reference signal in the network elements output clock the value equal to the phase difference that remains after the phase

locked loop has acquired the new frequency of the reference signal. See column 5, lines 35-50.

From the above, it is clear Powell also is not interested, motivated, or does not teach or suggest anything at all to do with wander or jitter or two separate and distinct filters for the same purpose.

It is further submitted the Examiner is using hindsight to arrive at applicants' claimed invention with the applied art of record. The Examiner is using the limitations of applicants' claims as a road map to find all the different limitations in different references, and having done so concludes that applicants' claimed invention is arrived at. Here, not only is hindsight being used, but the limitations being interpreted as existing, are not actually identified in the prior art.

Additionally, the Examiner cannot take the teachings out of the context in which they are found. The context of Sutardja and Powell have nothing to do with each other and are not combinable. Powell specifically teaches an optical network, while Sutardja teaches a standard electrical circuit and network. The total purpose and design of Sutardja is for a type 1 timing circuit to act as a type 2 timing circuit. Powell has nothing at all to do with this and in contrast is concerned with achieving fast pulse settling during the clock hold over recovery period in a synchronous optical network. One has nothing to do with the other. Applicants have no idea how to take the teachings of Powell when a relatively significant

change in the frequency of the reference signal occurs and is somehow or other applied to the architecture taught by Sutardja which has no need or concern of the same. Moreover, this has nothing at all to do with applicants' claimed invention regarding jitter and wander. To even try to figure out how to accomplish such a combination will require undue experimentation and research, which only further supports the non obviousness of applicants' claimed invention and the inability to combine the applied art of record.

It must also be mentioned that the law requires there must be some teaching or suggestion in the references themselves to combine the teachings the Examiner is relying upon to arrive at applicants' claimed invention. Here, there is no teaching or suggestion whatsoever to combine the teachings of Powell with Sutardja for the purposes the Examiner is relying upon to arrive at applicants' claimed invention.

Lastly, to the extent that the Examiner relies on the Sonet requirements that were put forth in the late 1980's, there is no teaching or suggestion of the limitation of "a second filter for removing wander from the signal separate and apart from the first filter". This specific limitation of the second filter being separate and apart from the first filter is nowhere to be found. Moreover, the context is totally distinct from the primary reference, Sutardja, and again, there is no teaching or suggestion to combine such teachings. Accordingly, it is respectfully submitted the applied art of record does not teach or suggest the limitations of Claims 1-4 and 16, these claims are patentable over the applied art record.

In regard to the rejection of Claims 25 and 26 as being unpatentable over Bedrosian in view of Sutardja and further in view of Powell, it is respectfully submitted that Bedrosian adds nothing to the relevant teachings discussed above in regard to Sutardja and Powell. For the reasons explained above in regard to Sutardja and Powell, Claims 25 and 26 are patentable over the applied art record.

The Examiner has objected to Claims 5-13 and 17-23 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In view of the foregoing remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-13, 16-23 and 25-27, now in this application be allowed.

Respectfully submitted,

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